大师高级课程系列之

10-200Gb/s串行解串器设计实现千兆位连接

10-to-200 Gb/s SerDes Design Enabling Terabit Connectivity

2023 年11月09日– 10日 | 上海

一、为什么参加：

在过去的20年里，互联的技术发生了翻天覆地的变化。中速SerDe(1-32 GB/S) 的能效越来越高，以满足面向机器学习（ML）的硬件开发日益增长的需求。与此同时，从 56 Gb/s 到 200+ Gb/s，均衡和定时恢复技术都采用了基于 ADC-DAC-DSP 的数字方法。当今 SerDes 设计人员面临的挑战是如何同时适应这两种架构和调制方案。本期短期课程旨在通过提供 SerDes 空间所需的系统级和电路级概念来弥补这些差距。本短期课程将从传统的模拟架构开始，逐步发展到今天基于 DSP 的均衡和定时恢复。本课程从传统的模拟混合信号 SerDes 架构开始，该架构如今仍适用于 UCI、HBM 和 XSR 解决方案。之后，我们将转向 ADC-DSP 解决方案。ISI 和延迟在当今基于 DSP 的接收器中发挥着重要作用，尤其是在多级信号方面。本短期课程将包括数字均衡、定时恢复、它们之间的相互作用和相互依存关系。此外，还将介绍基于 DSP 的均衡的最新趋势 MLSD。

Over the last 20 years, the landscape of Interconnects has evolved drastically. The mid-speed SerDes (1-32 Gb/s) are becoming more energy efficient to keep up with the growing demand to meet machine learning (ML) oriented hardware development. At the same time, 56 Gb/s to 200+ Gb/s, equalization, and timing-recovery techniques have adopted ADC-DAC-DSP-based digital approach. The challenge for today's SerDes designers is aligning themselves to both architectures and modulation schemes. This short course aims to bridge those gaps by providing both systems-

level and circuit-level concepts necessary for SerDes space. Starting from traditional analog architectures, this short course will walk through the evolution toward today's DSP-based equalization and timing recovery. The short course starts from traditional analog-mixed signal SerDes architecture that is still relevant today for UCI, HBM, and XSR solutions. Following that we will move towards ADC-DSP solutions. ISI and latency play a significant role in today's DSP-based receivers, especially with multi-level signalling. This short course will include digital equalization, timing recovery, their interaction, and interdependency. MLSD, a recent trend in DSP-based equalization will also be covered.

二、谁应该参加

有经验的模拟集成电路设计人员，希望加深对高速串行接口设计中信号的了解，并向该领域的世界级专家学习。

Experienced analog IC designers, who wish to deepen their knowledge about signaling in high-speed serial interface design and learn from a world-class expert on this topic.

三、课程主办单位：

上海林恩信息咨询有限公司

上海集成电路技术与产业促进中心

四、课程安排

课程时间：2023年11月09日—10日 （2天）

报到注册时间：2023年11月09日， 上午8:30-9:00

课程地点：上海集成电路技术与产业促进中心（上海市浦东新区张东路1388号21幢）

五、课程注册费用

课程注册费用 4600 元/人（含授课费、场地租赁费、资料费、课程期间午餐），学员交通、食宿等费用自理（报名回执表中将提供相关协议酒店信息供选择）。优惠折扣：在校学生注册费用 3600 元/人；

4 人以上团体报名优惠可协商；

报名方式请各单位收到通知后，积极选派人员参加。报名截止日期为 **2023 年 11 月 07 日**，请在此日期前将报名回执表发送 Email 至：

邮件：steven.yu@lynneconsulting.com 报名咨询电话：021-58978665；或者添加微信：136 7161 3108（手机），暗号：SerDes 课程。关于付款：请于 11 月 07 日前将全款汇至以下账户。并备注（SerDes 课程+单位/学校+姓名）

银行信息：户　　名：上海林恩信息咨询有限公司开户行：上海银行曹杨支行帐　　号：31658603000624127

支付宝信息：公司名称：上海林恩信息咨询有限公司支付宝账号：steven.yu@lynneconsulting.com

六、课程具体安排

2023年11月09日—10日　（两天）

Day: 1 Analog mixed signal SerDes

1. Channel Response, Modulation, ISI and Equalization, Design and Implementation.

2. Timing recovery techniques.

3. Transceiver Receiver Architecture choices

Test case: I A 40 Gb/s long reach SerDes Design

Test case: II A 25 Gb/s energy-efficient PAM-3 link for ML applications

Day: 2　DAC-ADC-DSP based SerDes

1.　DSP-DAC based Transmitter

2. ADC-DSP based Receiver

3. Equalization, Adaptation, and advanced modulation

Test case: III ADC-DSP based 112 Gb/s Long reach SerDes in 7nm finFET

Q&A: Related Problems faced by Participants

七、教授简介

Masum Hossain 教授专家简介：

专家简介：

Masum Hossain 于 2010 年获得多伦多大学博士学位。在此之前，他分别于 2002 年和 2005 年获得孟加拉国工程技术大学理学士学位和皇后大学理学硕士学位。2013 年冬季起，加入阿尔伯塔大学电气与计算机工程系任教，担任助理教授。最近于2023年加入加拿大渥太华的卡尔顿大学。

在重返学术界之前，Masum Hossain 曾在工业研究领域工作过数年。2007 年 9 月至 2008 年 1 月，他在英特尔电路研究实验室（CRL）实习。2008 年至 2010 年，他在 Gennum 公司的模拟和混合信号部门工作，主要负责开发世界上容量最大、功耗最高的交叉点路由器解决方案。之后，Masum Hossain 加入 Rambus 实验室，担任高级技术人员。在 Rambus，他的研究重点是高速接口的高级均衡和时钟恢复技术。他的研究兴趣包括高速芯片到芯片通信的混合信号电路、均衡和时钟恢复技术。

Masum Hossain 在 2008 年 IEEE 定制集成电路（CICC）会议上获得最佳学生论文奖。2010 年，他还获得了 Analog Device 的杰出学生设计师奖。2021 年，他获得 EPS Society 提名的 IEEE Transaction in Components, Packaging and Manufacturing 最佳论文奖。

Masum Hossain received his Ph.D. at the University of Toronto in 2010. Prior to

that, he received a B.Sc. Degree from the Bangladesh University of Engineering and Technology, and an M.Sc. degree from Queen's University, in 2002 and 2005, respectively. Since winter 2013, I joined the faculty of the University of Alberta Department of Electrical and Computer Engineering as an Assistant Professor. Recently in 2023, he joined Carleton University in Ottawa, Canada.

Before returning to academia, Masum Hossain has spent several years in industrial research. From September 2007 to January 2008, He was a graduate intern with Intel Circuit Research Lab (CRL). From 2008 to 2010, he was with Gennum Corp. in the Analog and Mixed Signal division where he focused on the development of the world's highest capacity and most power efficient cross point router solution. Following that, Masum Hossain joined Rambus Lab as a senior member of technical staff. At Rambus, his research focused on advanced equalization and clock recovery techniques for high-speed interfaces. His research interests include mixed-signal circuits for high-speed chip-to-chip communications, equalization, and clock recovery techniques.

Masum Hossain won the best student paper award at the 2008 IEEE Custom Integrated Circuits (CICC) Conference. He also won Analog Device's Outstanding Student Designer Award in 2010. In 2021 he received EPS Society nominated best paper award in IEEE Transaction in Components, Packaging and Manufacturing.