ESD 保护设计研讨会--
绝缘硅(SOI)和物联网(IOT)

（13:00pm-16:00pm,16th Step. 2015）

Seminar Venue： Building 21, No 1388, Zhangdong Road, Pudong New District, Shanghai, China

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The Seminar Schedule: -- Free registration!!(13:00pm-13:30pm)

Part 1: ESD protection design in SOI (13:30pm-14:30pm)

- Introduction
- Challenges for ESD protection of SOI circuits
- Solutions (public and Sofics)
- Question/answer session

Abstract:

Recently, advanced SOI technology nodes are being used more extensively due to a number of advantages mainly related to the reduction of the power consumption, smaller silicon area, shorter gate delay and reduced parasitic junction capacitance. Moreover, due to the completely isolated transistors, latch-up is no longer an issue.

However, SOI technology comes also with disadvantages such as the higher cost for the starting material, floating body and history effects, increased self-heating issues and a higher design complexity. Another main disadvantage is the fact that traditional ESD concepts have a much reduced (It2) failure current. This reduction compared to bulk CMOS is related to the thin silicon film and the complete isolation of the transistors which limits the dissipation and transfer of the generated heat. The MOS devices are very sensitive against ESD stress, not only for gate-to-source stress but also for drain-to-source stress. Even a forward diode, a key element for many ESD concepts, has a much lower robustness as compared to bulk CMOS.

This presentation will provide information about ESD concepts that have been successfully applied in SOI CMOS technology, including low resistive diodes with improved ESD-performance-per-area, self-protective MOS drivers through various layout concepts. Examples from several sources will be summarized. Finally, the presentation will cover a layout method to create Silicon Controlled Rectifiers which can provide a very area efficient solution for many ESD challenges.

Part 2: ESD protection design in IoT(14:45pm-15:45pm)

- Introduction
- Reliability challenges for IoT
- Solutions (public and Sofics)
- Question/answer session

Abstract:

When thinking about IC design at mature nodes that exist for more than 20 years (like 180nm), one would argue that the foundries have covered every aspect of Electrostatic Discharge (ESD), Electrical Overstress (EOS) and Latch-up long ago. However, what we have learned by supporting those innovative startups is that many of the applications in IoT require non-standard on-chip ESD protection clamps for a number of reasons.

Several IoT systems include sensor or actuator interfaces that come with distinctive signal conditions. E.g. the driving voltage of the implanted chip to restore hearing for (near) deaf people is in the order of 20V, much beyond the typical I/O interfaces provided by the foundry or I/O providers. Similarly, small signals (order of a few mV or mA) captured by sensors for motion detection and touch remain hidden in the noise or are lost due to leakage created by General Purpose Input Output circuits (GPIO).

Every (innovative) system needs to communicate with its surroundings or directly with 'the internet'. Therefore wireless interfaces and/or high speed digital connections can be found on almost all of the systems. For both (wireless, wired) the IC designer needs on-chip ESD protection with low parasitic capacitance (200fF or lower). This means that most of the general purpose interface circuits provided by the foundry are not suitable and alternatives have to be created.

A lot of the innovative systems are meant to be low-cost and mobile and also this relates to ESD in several ways. To reduce the size of the system and the Bill of Materials (BOM), system designers are removing board level ESD protection blocks from the mini-Printed Circuit Boards (PCB). These Transient Voltage Suppressors (TVS) devices were added on PCBs 20 years ago to protect ICs against ESD stress during the actual use of products. Without those TVS-blocks and due to the much shorter PCB traces Integrated Circuits are stressed with more severe ESD stress like IEC 61000-4-2. This has a factor of 4 to 5 higher stress current compared to component level Human Body Model (HBM) ESD.

Moreover, the probability of ESD stress is much higher in those mobile systems as they are operated in so-called harsh environments. One just recalls the engineering course on electrostatics to consider that plastic (e.g. smartphone cover) rubbed by cloth (your back-pocket) generates a lot of charges - just millimeters away from the high speed USB port.

So even on-chip ESD protection can be considered as a way to make it hard for other companies to quickly replicate the functionality. This presentation will discuss the challenges and present solutions.

Who Should Attend：

This seminar has been developed for several categories of designers:

- Managers of design teams of ESD/EMC, analog IP blocks and circuits, and their designers.
- ESD Specialist/Engineer、 Engineers correlated with Engineering/Quality、System Engineer
- Designers with ESD experience, to update their ESD knowledge and to tune their experience to the present-day design procedures.

Why Lynne Consulting：

Lynne Consulting is offering advanced engineering courses in the field of analog, RF and mixed-signal IC design targeting the audience of electrical engineers, company managers and marketing engineers working in the semiconductor industry. The lecturers are leading practitioners and top experts in the area from high-technology companies and universities, who teach the most up-to-date information available at the time of the course.

Registration Method：

- **Free registration: Please fill out the registration form（in the attachment）and send the completed form to：**

Email：service@lynneconsulting.com
Fax: 021-3327 5892

Lecturer's Biography:

Bart Keppens received an Engineer degree in Electronics in Leuven in 1996. His master thesis, together with his colleague Steven Servaes, 'Transmission Line Pulsing (TLP) technique for analyzing ESD reliability', performed at IMEC, Leuven, Belgium, received the BARCO-award for best Industrial Engineer thesis in 1996. In 1996 Bart joined IMEC and was responsible for device electrical characterization, support for the ESD group and for the Non Volatile Memories group for layout and testing.

From May 2002 he joined Sarnoff Europe, Belgium, solving ESD related problems for customers worldwide, first as ESD engineer, later as technical leader, ESD design specialist. From 2006, Bart supports the Business Development initiatives as Technical Director for ESD. After a management buy-out in June 2009, Sarnoff Europe became 'SOFICS - Solutions for ICs' where Bart is Director Technical Marketing working with semiconductor companies worldwide.

Bart (co-) authored more than 25 peer-reviewed published articles in the field of 'on-chip ESD protection and testing' and 'Non Volatile Memories'.

Invited papers on ESD solutions and TLP analysis techniques have been delivered at the RCJ ESD symposium in Japan every year between 2006 - 2012. He is member of the Technical Program Committee ('TPC') of the EOS/ESD symposium since 2003, member of the ESREF TPC in 2003, 2005, 2007, 2009 and 2010 and member of the Taiwan ESD and Reliability conference TPC since 2010. Bart acted as a Workshop Panelist on ESD topics during various conferences (EOS/ESD Symposium and RCJ) and presented invited tutorials at Taiwan ESD and Reliability conference in 2008, 2010 and 2012. Bart holds several on-chip ESD protection design patents.

Sofics is IP alliance partner and Design Center Alliance partner with **TSMC**. Our have solutions verified on every node from **0.35um CMOS to 28nm**. Our are already working on a first test chip in **16nm FinFET**.

Sofics is an IP partner of **UMC**. We have solutions verified on **180nm BCD, 130nm, 65nm and 28nm**

Sofics has supported customers on **SMIC 90nm** and **Grace Semi 130nm.**

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ESD 保护设计研讨会注册报名表

研讨会时间安排：2015年09月16号，下午：13:30-16:00

单位名称				
通信地址			邮 编	
单位联系人				
姓 名	职 务	电 话	手 机	电子邮箱
参加研讨会人员名单				
姓 名	职 务	电 话	手 机	电子邮箱
参加人数共计： 人				

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