CWCM
2015
10th-12th June
Shanghai

第二届紧凑型器件建模研讨会

2nd China Workshop on Compact Modeling (CWCM 2015)

（10th-12th June 2015）

Why Participate：

The aim of the Compact Modeling workshop 2015 is to bring together a large group of people working at the frontiers of compact modeling design to study and discuss possibilities and future developments.

Model is the core value of circuits design, in the actual semiconductor environment, due to the increasing cost in both manufacturing and design for most advanced technology nodes, a real knowledge gap leads to multiple expensive design iterations, which penalize both customers and suppliers in terms of product prices. This discrepancy is even more amplified in the actual semiconductor supply chain where the manufacturing and design activities are completely disconnected (eg, pure play foundries and fabless design houses). Device model, as the bridge between foundry and design houses, this workshop provides a platform for both sides to discuss trends of model development and how to close the gap between design houses and foundries. Through gap filling and know-how exchange, design houses can have products with more additional value, foundry can deliver perfect support for design houses through intimate communication.

The workshop provides an opportunity for the discussion and the presentation of advances in compact modeling design of integrated circuits, especially in the field of RF circuits design, reliability and III-V devices. Presenters of this workshop are involved in the device modeling very long time and with lots of experience. It is a good chance to have a face to face discussion with these experts and learn from each other.

Who Should Attend：

This workshop has been developed for several categories of designers:

- Managers of design teams of Modeling, analog circuits, RFIC and their designers.
- Device (modeling) engineer, Spice modeling Engineer, Analog IC Design /RF IC Design engineer.
- Designers with compact modeling experience, to update their compact modeling knowledge and to tune their experience to the present-day design procedures.

Why Lynne Consulting：

Lynne Consulting is offering advanced engineering courses in the field of analog, RF and mixed-signal IC design targeting the audience of electrical engineers, company managers and marketing engineers working in the semiconductor industry. The lecturers are leading practitioners and top experts in the area

from high-technology companies and universities, who teach the most up-to-date information available at the time of the course.

Program Schedule:

Tutorial #1

"Development of High Performance Monolithic Spiral Inductive Devices: from the Layout Design to the Model"

Dr. Raphael Valentin,
XYTECH Consulting Founder&Technical Director

Title：Development of High Performance Monolithic Spiral Inductive Devices: from the Layout Design to the Model

Abstract: Monolithic spiral inductors and transformers play a crucial role in radio frequency integrated circuits (RF ICs) as low noise amplifiers, power amplifier, mixers, voltage controlled oscillators, and so on. These components are utilized to implement on-chip matching networks, passive filters, inductive loads, transformers, baluns, and so on. As silicon technology gradually dominating the RF IC market, the rising demand for high quality monolithic spiral inductive devices has led to a significant progress in the silicon-based monolithic spiral inductors design techniques. Exhibiting low production fluctuation, good matching, they are also attractive for commonly used differential architectures. In addition, monolithic spiral inductive devices permit a large range of inductances and inductive behavior to be realized by changing simply the geometry or the shape. Unfortunately, it is true that by using thin copper and/or thin aluminum metal layers, incorporated into a sandwich of disparate, dielectrics, posed usually on a lossy silicon substrate, monolithic spiral inductive devices are subject to many parasitic effects. As a drawback, they are responsible of the degradation of the quality factor. Moreover, because these parasitic effects correlate each other along the path line, monolithic spiral inductive devices are also difficult to model.

In a first part, we will relate about the design of dedicated/non-conventional monolithic spiral inductive devices featuring higher performances, lower area consumption, and reduced cross-coupling. Based on simple hand calculations, electromagnetic simulations and simple considerations, few interesting shapes and geometries of planar, stacked, eight-shaped inductors and transformers will be explored. In addition, we will discuss about the impact of the so-called ground patterned shield on the performances of the inductive devices.

In a last part, we will discuss about the development of small electrical circuit models of inductive devices for integration in a standard circuit design environment (such as SPICE). First, based on simple hand calculations, we will describe explicitly an equivalent scalable circuit representation of the skin effects using the Maxwell's equation based intrinsic impedance expression. After, we will highlight how the model accuracy of inductive devices can be improved when a distributed small electrical circuit representation is used. As benches, few test

cases when applying different realistic impedances to the ports will be presented. Finally, we will illustrate the level of accuracy of our improved models.

Biography：

Dr. Raphael Valentin received the Ph.D. degree in micro and nanotechnologies from the Institute of Electronics, Microelectronics and Nanotechnology (IEMN), Villeneuve d’ Ascq,France, in 2008. His Ph.D. degree research was on the device simulation/modeling and measurement of the nano-scaled Metallic Source/Drain Fully Depleted SOI transistors dedicated to high-frequency applications. He was working as Post Doc CEA LETI at ST Microelectronics in the Modeling Group. His main research interest concerned advanced radio frequency (up to 100 GHz) Compact Modeling of SOI CMOS devices dedicated to high speed/low power communications. He worked at Montage Tech, Inc, responsible for the Device and Modeling activities at Shanghai. Based on his experiences, he found XYTECH Consulting Ltd. in order to provide expertise and resources for Integrated Circuits (IC) Industries and related area, focusing on the technical topics related to the development of improved and dedicated semiconductor devices.

Tutorial #2

“Modeling of Transistors in CMOS Radio Frequency and Microwave Integrated Circuits”

Prof. Yan Wang，
Tsinghua University

Title：Modeling of Transistors in CMOS Radio Frequency and Microwave Integrated Circuits

Abstract: With the rapid advancement of CMOS process technology, transistor performance at high frequency band has improved drastically. Thus, the adoption of CMOS in radio and microwave integrated circuits (RF/MWIC) becomes possible and promising. However, challenges still exist due to the relatively inferior devices quality caused by substrate. Lack of high quality devices results in tight design margin and need for very precise models in order to exploit the full process potential. Yet the devices and components modeling still lags behind the pace of circuits design. This talk is mainly devoted to signal equivalent circuit model and large signal equivalent circuit model of CMOS transistors. Firstly, an improved small signal model for transistors has been proposed with parameter extraction flow for both parasitic and intrinsic effects respectively, which agrees with measured high frequency multi-bias S-parameters very well. Secondly, a large signal model based on a BSIM4 core model and extended by parasitic sub-circuit model with complete flow of parameter extraction is developed, which accurately predicts DC, multi-bias S-parameters and load-pull large signal data. Thirdly, a scalable modeling strategy using pre-modeled cell transistors is developed, allowing scalable gate width，and is validated to be able to simulated transistor small signal performance across wide range of sizes.

Biography：

Prof. Yan Wang received the B.S. and M.S. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 1988 and 1991, respectively, and the Ph.D. degree in semiconductor device and physics from Institute of Semiconductors, the Chinese Academy of Sciences, Beijing, China, in 1995. Since 1999, she has been a Professor with the Institute of Microelectronics, Tsinghua University (IMETU), Beijing. Her current research interests include modeling of transistors and components, the carrier transport models in scaled-down MOS devices, CAD software development for micro- and nano-devices.

Tutorial #3

"Simulation and Analysis of Single-Event Effects and Soft Errors"

Dr. Shen Chen，
CTO of Cogenda

Title： Simulation and Analysis of Single-Event Effects and Soft Errors

Abstract: Single-event effects (SEE) induced by energetic particles are the primary cause of soft errors in integrated circuits. With the technology scaling, transistors are becoming more sensitive to single-event effects and soft error is a growing concern in IC reliability. TCAD device simulation and Monte-Carlo particle simulation are well-known for their ability to reveal the physical mechanisms behind SEE. In this talk, we will first introduce the radiation sources relevant to the soft errors in space and ground environments and the essential physical processes in an SEE event. This will be followed by an elaboration of simulation techniques to study SEE and simplified engineering models to predict soft error rates. Finally, we will provide two realistic examples:

- Estimation of single-event upset and latchup in SRAM cell and array;
- Optimization of radiation-tolerant D-flipflops in a cell library;

Biography：

Dr. Shen Chen was with Silicon Nano Device Laboratory of National University of Singapore between 2004 and 2009, where his research involves reliability physics, device physics of novel switching and memory devices and numerical simulation. He received his Ph.D. from NUS in 2009. He has authored or co-authored over 40 peer-reviewed papers at international journals and conferences including the IEEE EDL, TED, IEDM and IRPS. He serves as regular reviews to two of IEEE journals.

In 2008 and 2011, Dr. Shen co-founded Cogenda Pte Ltd in Singapore and Cogenda Co Ltd in Suzhou, respectively, which supply numerical simulation software and technical support to the microelectronics industry. His recent effort focuses on the studying of radiation effects and radiation-harden-by-design

techniques. He managed the development of a series of software in this field, including VisualTCAD the device simulator, VisualParticle the particle simulator and McSEE the single-event effects analysis tool.

Tutorial #4

"PSPSOI Model solution for RF-SOI Technology"

Sunny Zhang,
Department Manager of HHGrace

Title： PSPSOI Model solution for RF-SOI Technology

Abstract: SOI technology has now emerged as a strong contender in the high performance RF switch market, offering lower insertion loss, better noise isolation characteristics and linearity. An accurate SOI compact model is fundamental for RF design. The model should includes accurate modeling of floating body effect, parasitic bipolar current, nonlinear body resistance, low and high frequency noise as well as higher order derivatives of current-voltage characteristics. HHGrace offered customers PSP-SOI model solution with accurate description of above performance, valid from DC to Radio Frequency, can be applied for both small and large-signal analysis. The model and PDK had been verified in 0.20um SOI technology with several products.

HHGrace: Shanghai Huahong Grace Semiconductor Manufacturing Corporation ("HHGrace"), incorporated through the consolidation between Shanghai Hua Hong NEC Electronics Company, Limited ("Hua Hong NEC") and Grace Semiconductor Manufacturing Corporation ("Grace"), has become one of the world's leading 200mm pure-play wafer foundries. With three 200mm wafer fabrication facilities in Zhangjiang and Jinqiao of Shanghai, HHGrace offers production capacity over 129,000 200mm wafers per month. HHGrace provides professional and highly value-added foundry services covering technology solutions from 1.0μm to 90nm process nodes, focusing on differentiated technologies including eNVM (embedded Non-Volatile Memory), power management IC, power discrete, RF, as well as standard logic and mixed-signal. HHGrace is also in the process of developing MEMS solutions as one of its up-and-coming technologies. With its headquarters located in Shanghai, China, HHGrace extends its sales and technical supports to customers in Taiwan, Japan, North America and Europe. For more information, please visit http://www.hhgrace.com.

Tutorial #5

"Advanced RF Device Modelling cum IC Validation"

Prof. Fujiang Lin，
University of Science and Technology of China

Title：Advanced RF Device Modelling cum IC Validation

Abstract: It is well-known that any RFIC simulation can only as accurate as the device model can predict. Accountable model and library are therefore the bottleneck for the effective 1st time MMIC/RFIC/mmW-IC design success. High cost of modern process technology and reliable EDA tools have pushing traditional RF modelling paradigm shifted. New modelling approach and methodology, in particular for advanced technology and/or devices have emerged. In this talk, some overview and new development trends, based on lecturer's decades' hand-on experiences on variable technologies will be presented.

- RF modeling paradigm shift;
- Measurement, characterization and calibration;
- Scalable RF package modeling;
- CAD oriented III-V large-signal modeling;
- SiGe modeling;
- RF CMOS modeling;
- RF noise and 1/f noise modeling;
- GaN modeling;

Biography：

Prof. Fujiang Lin, male, born in 1958, currently works as a professor and doctoral supervisor at the School of Information Science and Technology, University of Science and Technology of China (USTC). Lin is a scientist in the field of microwave / microelectronics. In 2010, Lin was selected into the list of candidates of the Recruitment Program of Global Experts of China also called the "Thousand Talents Program". Under such a program, Lin was introduced from Singapore to work at USTC. Prof. Lin is currently the Executive Director of the Department of Electronic Science and Technology, USTC.

Lin was enrolled into the Department of Radio Electronics of USTC in 1977, the year when the suspended National College Entrance Exam was resumed in China. Lin received his B.S. and M.S. degrees from USTC in 1982 and 1985 respectively. In 1986, Lin was sent to Germany for further study sponsored by the government. In 1993, Lin received his Ph.D. from the University of Kassel, Germany. In 1995, he joined the Institute of Microelectronics (IME), Singapore, as a Member of Technical Staff, where he pioneered practical RF modeling for RF integrated circuit (IC) development. In 1999, he joined HP EEsof, as the Technical Director, where he established the Singapore Microelectronics Modeling Center, providing accurate state-of-the-art device and package characterization and modeling solution service worldwide. From 2001 to 2002, he started up and headed Transilica Singapore Pte. Ltd., a research and development design center of Transilica Inc., a Bluetooth and IEEE 802.11 a/b wireless system-on-chip (SoC) company. In 2002, he joined Chartered Semiconductor Manufacturing Ltd., as Director, where he led the SPICE modeling team in support of company business. In 2003, he re-joined IME, Singapore as Senior Member of Technical Staff and Principle Investigator for upstream R&D initiative and leadership towards NANOELECTRONICS - THE NEXT WAVE.

Prof. Lin has long been engaged in cross-disciplinary research on microwave / microelectronics, being an influential scholar in this field internationally. Prof. Lin has served IEEE activities in different functions since 1995 including chair of the Singapore Microwave Theory and Techniques (MTT)/Antennas and Propagation (AP) Chapter, reviewer board member for the IEEE Microwave Theory and Techniques Society (MTT-S), and

Technical Program Committee (TPC) member of RFIC. He is the initiator and co-organizer of series IEEE international symposium, workshops and short courses such as Radio-Frequency Integration Technology (RFIT). He was the recipient of the 1998 Innovator Award presented by EDN Asia Magazine. Prof. Lin has authored or coauthored over 100 scientific papers. He also jointly holds five patents.

Tutorial #6

"S-parameter and Non-linear RF modeling"

Dr. Franz Sischka,

CEO of Sisconsult & XMOD consultant

Title： S-parameter and Non-linear RF modeling

Abstract: The modeling of electronic devices means to describe their currents and charges by mathematical equations, as a function of applied DC biasing, applied RF test signals, operating temperature and for scaling models, very often also as a function of its geometry.

While passive devices like resistors, capacitors and inductors behave linear, i.e. their characteristics are independent of the applied measurement power, devices like diodes and transistors behave non-linear. In the DC range, non-linear currents are measured as functions of applied voltages, and have to be modeled, i.e. fitted. For higher frequencies, S-parameters are used to model the charges. However, S-parameters, measured by vector network analyzers, are linear and therefore, require that the applied RF test signal stays quite small to keep the non-linear device behaving linear, at the selected DC operating point. Nonlinearities, as a function of applied RF power, are not covered.

But in many modern applications, the operation range of diodes and transistors is in the Milli-Watt and even the in the Watt range, far above the required low RF signal level of S-parameters. To also cover this application range, non-linear network analyzer measurement and modeling comes into play. This allows measuring and modeling both, magnitude and phase of RF power sweeps, for the fundamental frequency and its harmonics, as a function of the RF signal level.

Since device models are only as good as the underlaying measurements, this lecture will also explain ways to verify the quality of the obtained measurements, before doing the device modeling.

Biography：

Dr. Franz Sischka studied communication engineering at the University of Stuttgart, Germany, where he received his Diplom-Ingenieur and Ph.D. degrees in 1979 and 1984. He joined Hewlett-Packard in Boeblingen/Germany, working in R&D in the fiber optics group. Since 1989, he became a consultant for Hewlett-Packard's, later Agilent-EEsof's device modeling software IC-CAP. During that time, he has focused on developing strategies for verified, reliable device measurements and also worked on modeling strategies for diodes, bipolar and GaAs transistors, as well as for passive components like spiral inductors, varactors etc.

He is the author of Agilent's (now Keysight's) IC-CAP Modeling Handbook.

Short Course Detail:

Short Course

"Device Measurement and Verification"

11st-12th June 2015

By Dr. Franz Sischka

Theme 1: DC Measurements

- Challenges
- Data Verification

Theme 2: CV Measurements

- Applying LCRZ Meters

Theme 3: S-Parameter Measurements

- Direct Interpretation of S-Parameter Measurements
- Guide for Verified S-Parameter Measurements

Theme 4: 1/f Noise

- Measurements and Data Verification

Theme 5: Parameter Extraction Techniques

- Regression Analysis
- Visual Parameter Extraction

Theme 6: Fundamentals of Device Modeling

- Diode (DC -> CV -> S-parameter -> nonlinear RF)
- HEMT Transistor Modeling (Angelov)
- Passive Device Modeling: model development
- based on measurement results

Registration Information:

Registration Category	Tutorial (10th,June)	Short Course (11st-12th,June)	Both Tutorial and Short Course (10th-12th,June)
Regular	RMB 800	RMB 2800	RMB 3300
Student	RMB 500	RMB 2000	RMB 2200

Discount： A 10% discount applies for groups（3 persons or more）

The Registration Fee Includes:

- Access to workshop materials (in appropriate format)
- Tea, coffee and lunch throughout the workshop

Bank Account Information:

- Beneficiary: 上海林恩信息咨询有限公司/Lynne Consulting (Shanghai) Co., Ltd
- Bank: 上海银行曹杨支行/Bank of Shanghai Caoyang Branch
- Account No.: 316586 03000624127(收款账号)
- Registration Due：**3rd June 2015**

Organizing Committee:

Organization（listed at random）：

- 上海林恩信息咨询有限公司/Lynne Consulting (Shanghai) Co., Ltd
- 杭州电子科技大学/HANGZHOU DIANZI UNIVERSITY
- 上海集成电路技术与产业促进中心/Shanghai IC Technology & Industry Promotion Center
- 弘模半导体技术(上海)有限公司/ XMOD Technologies

Organizers：

- 上海林恩信息咨询有限公司/LYNNE CONSULTING

Workshop Venue：

上海市浦东新区张东路 1388 号 21 栋/Building 21, No 1388, Zhangdong Road, Pudong New District, Shanghai, China

Registration Method：

Please fill out the registration form（in the attachment）and send the completed form to：

- Email：steven.yu@lynneconsulting.com
- Fax: 021-33275892