CMOS 集成电路 ESD 防护设计课程-

Advanced ESD Protection Design in CMOS Integrated Circuits

（6th May 2015）

Why Participate：

The course will provide an overview of the typical issues designers face when they want to protect their circuits against Electrostatic Discharge. Through a set of basic and advanced case studies different on-chip ESD protection concepts are compared.

IC designers continue to combine ever more features in advanced digital Systems-on-Chips (SoCs) like analog to digital and digital to analog conversion, sensor interfaces, audio/video handling, high speed interfaces, optical links... The design of these circuits is complex and involves combining IP blocks from different sources.

On top of this functional design complexity, circuit designers face challenges related to ESD protection: on-chip ESD concepts used in general purpose I/O's are not well suited for many specialty interfaces because they introduce high parasitic capacitance, series resistance and leakage current. Similar problems exist in BCD platforms for automotive applications and other high voltage applications. E.g. the amount of electronic circuits in cars has been steadily increasing to an average of more than 50 ASICs per car. Not only the number of circuits in cars has been expanding. Also the quality requirements have been continuously increasing. While on-chip ESD requirements are being lowered in consumer electronics the specifications for automotive parts have only been increased. LIN/CAN interfaces for instance must pass stringent system level ESD stress (IEC 61000-4-2) of more than 6kV. This increased requirement strongly limits the options for ESD protection. Furthermore there are many non-ESD requirements that affect the selection of the most appropriate ESD concept: Electrical OverStress (EOS), Electromagnetic compatibility (EMC) and of course (transient) latch-up. Drastic changes to the process platform (SOI, 3D-IC, FinFETS) can also cause new ESD challenges.

Who Should Attend：

This course has been developed for several categories of designers:

- **Managers of design teams of ESD/EMC, analog IP blocks and circuits, and their designers.**
- **ESD Specialist/Engineer、 Engineers correlated with Engineering/Quality、System Engineer**

- **Designers with ESD experience, to update their ESD knowledge and to tune their experience to the present-day design procedures.**

Why Lynne Consulting：

Lynne Consulting is offering advanced engineering courses in the field of analog, RF and mixed-signal IC design targeting the audience of electrical engineers, company managers and marketing engineers working in the semiconductor industry. The lecturers are leading practitioners and top experts in the area from high-technology companies and universities, who teach the most up-to-date information available at the time of the course.

Course Details：

- **Duration: 1 day（6th May 2015）**

Location：Building 21, No 1388, Zhangdong Road, Pudong New District, Shanghai, China

- **Fees:￥1200/person**

A discount applies for groups before 22nd April 2015 （2 persons（Total：￥2180）；3 persons（Total：￥3100）；4 persons or more（negotiation））

- **￥800/person for students**
- **The above discount can not apply simultaneously**
- **Online Registration(www.lynneconsulting.com)**
- **Contact us(Steven.Yu,021-58978665,Email:steven.yu@lynneconsulting.com)**

The Course Schedule:

THEME 1: Introduction

- Reason for On-chip ESD protection

THEME 2: ESD design window

- Concept
- ESD test models

THEME 3: ESD protection approach overview

- Device types
- Protection concepts

THEME 4: ESD protection for advanced CMOS

- Analog interfaces
- Advanced CMOS nodes
- High voltage tolerant interfaces
- Wireless interfaces
- High speed interfaces
- ESD protection in SOI processes
- Sofics approach and track records

THEME 5: ESD protection in high voltage, BCD

- ESD protection in high voltage
- Automotive, industrial applications
- Sofics approach and track records

THEME 6: Summary, conclusions

- Summary
- Trends
- Tools
- Conclusions

Lecturer's Biography:

Bart Keppens received an Engineer degree in Electronics in Leuven in 1996. His master thesis, together with his colleague Steven Servaes, 'Transmission Line Pulsing (TLP) technique for analyzing ESD reliability', performed at IMEC, Leuven, Belgium, received the BARCO-award for best Industrial Engineer thesis in 1996. In 1996 Bart joined IMEC and was responsible for device electrical characterization, support for the ESD group and for the Non Volatile Memories group for layout and testing.

From May 2002 he joined Sarnoff Europe, Belgium, solving ESD related problems for customers worldwide, first as ESD engineer, later as technical leader, ESD design specialist. From 2006, Bart supports the Business Development initiatives as Technical Director for ESD. After a management buy-out in June 2009, Sarnoff Europe became 'SOFICS - Solutions for ICs' where Bart is Director Technical Marketing working with semiconductor companies worldwide.
Bart (co-) authored more than 25 peer-reviewed published articles in the field of 'on-chip ESD protection and testing' and 'Non Volatile Memories'.

Invited papers on ESD solutions and TLP analysis techniques have been delivered at the RCJ ESD symposium in Japan every year between 2006 - 2012. He is member of the Technical Program Committee ('TPC') of the EOS/ESD symposium since 2003, member of the ESREF TPC in 2003, 2005, 2007, 2009 and 2010 and member of the Taiwan ESD and Reliability conference TPC since 2010. Bart acted as a Workshop Panelist on ESD topics during various conferences (EOS/ESD Symposium and RCJ) and presented invited tutorials at Taiwan ESD and Reliability conference in 2008, 2010 and 2012. Bart holds several on-chip ESD protection design patents.

About Sofics:

Sofics is the world leader in on-chip electrostatic discharge (ESD) and electrical overstress (EOS) solutions for ICs. Our technology is proven in all of the world's major foundries and process nodes, and has been successfully implemented in over a thousand chip designs from IC companies of all sizes.

Our TakeCharge portfolio of on-chip solutions offers unique advantages in any IC design requiring custom or specialty I/Os, from 0.18um down to 28nm. TakeCharge technology enables twice the I/O performance in applications that run at high frequencies or high speeds. In low-power applications it delivers ESD protection with leakage that is orders of magnitude lower than generic solutions. When applications call for more robust ESD/EOS protection, TakeCharge outperforms all other approaches while occupying far less silicon area.

Sofics also offers PowerQubic technology, a breakthrough in delivering robust on-chip EOS solutions in high-voltage applications. PowerQubic handles all system-level ESD/EOS requirements.

We also partner with other IC experts to develop integrated design solutions for specialized applications CustomIO. Sofics recently collaborated with ICsense to build a stable, fully ESD- protected I/O in both 40nm and 28nm that interfaces 1.8V gates with legacy 3.3V off-chip devices.

Sofics solutions are highly cost-effective. An IP license from Sofics is more economical than adding staff to an ESD department or hiring a consultant. It is also more cost-efficient than buying shuttle space to develop alternative solutions. Since our solutions are foundry and field-proven, licensees get IP that works the first time. This eliminates the need for expensive re-spins and gets the product to market faster.

With our large and growing portfolio of patented IP, in most cases the precise ESD/EOS solution you need will be available off the shelf. Our TakeCharge customers include many of the world's leading IC makers, and our PowerQubic portfolio has been licensed by a top tier foundry to offer to their customers.

Sofics is IP alliance partner and Design Center Alliance partner with **TSMC**. Our have solutions verified on every node from **0.35um CMOS to 28nm**. Our are already working on a first test chip in **16nm FinFET**.
Sofics is an IP partner of **UMC**. We have solutions verified on **180nm BCD, 130nm, 65nm and 28nm**
Sofics has supported customers on **SMIC 90nm** and **Grace Semi 130nm.**